Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-15. (cancelled)

16. (original) A method for evaluating an erase margin voltage in a single polysilicon EEPROM cell, said method comprising:

providing a memory circuit, comprising

an EEPROM cell having a control gate and an output node;

sweeping a voltage applied to said control gate through a range of voltages above about 0 V; and

determining from a signal on said output node when the margin voltage has been reached.

17. (original) The method of claim 16, wherein said voltage is swept upward from about 0 V.

18. (original) The method of claim 16, wherein said output node comprises a drain line.

19 . (original) The method of claim 16, wherein said output node further comprises a sense amplifier connected to said EEPROM cell by the drain line and a source line, said sense amplifier configured to detect margin voltages for said EEPROM cell.

20. (cancelled)

21. (new) The method of claim 16, wherein the memory circuit comprises:

a single polysilicon EEPROM cell having a drain line;

a margin test mode pull-up source device comprising two pull-up sources connected to said drain line, said margin test mode pull-up source device configured to produce an erase margin voltage of above 0 V in said EEPROM cell;

a sensor connected to said drain line configured to determine said erase margin voltage.

22. (new) The method of claim 21, wherein said margin test mode pull-up source device comprises an inverter.

23. (new) The method of claim 21, wherein said margin test mode pull-up source device comprises:

a p-channel transistor gate;

an inverter controlling said gate; and

a source line for said gate connected to Vcc.

24. (new) The method of claim 16, wherein the memory circuit comprises:

a single polysilicon EEPROM cell having a source line and a drain line;

a voltage control device comprising a transistor having a voltage control drain connected to the source line of the cell and a voltage control source connected to a node to which a p-channel transistor gate and an n-channel transistor gate are connected, connected to said source line, said voltage control device configured to produce an erase margin voltage of above 0 V in said EEPROM cell;

a sensor connected to said drain line configured to determine said erase margin voltage.

25. (new) The method of claim 24, wherein said voltage control device comprises a voltage control circuit configured to raise the source line bias voltage.

26. (new) The method of claim 25, wherein said voltage control circuit is further configured to raise the control gate bias.

27. (new) The method of claim 26, wherein said p-channel transistor and said n-channel transistor also have drains connected together and to the node.

28. (new) The method of claim 27, wherein said p-channel transistor has a source connected to V_{CC}, and said n-channel transistor has a source connected to ground.